DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] this invention relates to the circuit module which comes to mount the semiconductor device and this semiconductor device of the nakedness called a bare chip in the circuit board.
[0002]
[Description of the Prior Art] By electronic equipment like a portable computer, since a bulk memory is constituted, it has many semiconductor devices. Many electrodes are arranged at the periphery of the element side where the semiconductor device for the conventional memory faces the circuit board, and the LSI circuit is arranged to the field surrounded by these electrodes. And flip chip bonding of this semiconductor device is carried out to the circuit board.
[0003] By the way, in this kind of semiconductor device, since the LSI circuit is arranged to the field enclosed by the electrode, when a semiconductor device is miniaturized, it is in the inclination for the field of an LSI circuit to become narrow. The so-called semiconductor device of the LOC (lead on chip) structure which increased the field where the above-mentioned electrode is arranged side by side recently at a single tier in the center section of the element side, and an LSI circuit is arranged from this is known.
[0004] Since an electrode does not exist in the periphery of an element side, if the semiconductor device of LOC structure carries out flip chip bonding of this semiconductor device to the circuit board, it will become impossible to support the periphery of the element side of this semiconductor device, and it will become what has the unstable mounting posture of a semiconductor device. Therefore, after the semiconductor device which adopted LOC structure carries out wire bonding of the above-mentioned electrode to a leadframe, carrying out the mould of the whole with the resin for closure, and package-izing it as one module is performed.
[0005] and SOJ (Small OutlineJ-leaded Package) typical as a package for memory **** -- two or more leads are projected from the edges-on-both-sides section of a package, and these leads are soldered to the pad on the circuit board
[0006]
[Problem(s) to be Solved by the Invention] However, since the package of LOC structure is carrying out the mould of the semiconductor device by the resin for closure, it becomes what has the bigger configuration of a package than a semiconductor device. And since two or more leads have projected from the edges-on-both-sides section of a package, compared with the size of a semiconductor device, package size will become very big.
[0007] Therefore, the occupancy area of the package on the circuit board increases, and there is a problem of it becoming impossible to raise the packaging density on the circuit board. this invention is to obtain the circuit module which has the semiconductor device which was made based on such a situation, can carry out flip chip mounting easily at the circuit board though it is the composition which has arranged the electrode side by side at the single tier in the center section of the element side, and carries out suitable to high-density mounting, and this semiconductor device.
[0008]
[Means for Solving the Problem] The semiconductor device indicated by the claim 1 in order to attain the above-mentioned purpose is characterized by to have had the element side which faces the circuit board, to have been located in the above-mentioned element side at the both sides whose above-mentioned electrodes were pinched, while having arranged two or more electrodes directly joined to the above-mentioned circuit board by the center section of this element side side by side to the single tier, and to have arranged at least one support salient which touches the above-mentioned circuit board.
[0009] Since the support salient located in the both sides whose electrodes were pinched serves as a kind of pillar supporting a semiconductor device according to this composition, when a semiconductor device is mounted in the circuit board, the posture of this semiconductor device is stabilized. Therefore, flip chip bonding of the semiconductor device can be easily carried out to the circuit board, and high-density mounting can be realized.
[0010] According to the claim 2, the element side indicated by the above-mentioned claim 1 has four corners, and the support salient is arranged at these corners, respectively. According to this composition, since it is supported by the circuit board in four corners of an element side, the posture at the time of mounting a semiconductor device in the circuit board is stabilized more by the semiconductor device.
[0011] According to the claim 3, when the above-mentioned element side is seen superficially, the support salient indicated by the above-mentioned claim 1 has a relation which is located at a triangular vertex, and is arranged. According to this composition, since it is supported by the circuit board by three around an electrode, the posture at the time of mounting a

semiconductor device in the circuit board is stabilized by the semiconductor device.
[0012] According to the claim 4, the support salient indicated by the above-mentioned claim 1 serves as the function as an electrode. Since the number of the electrodes arranged in an element side increases according to this composition, the arrangement interval of the electrode arranged in the center section of the element side can be extended, and positioning and mounting to the circuit board can be performed easily.
[0013] In order to attain the above-mentioned purpose, the semiconductor device indicated by the claim 5 While arranging two or more electrodes which have the element side which faces the circuit board and are directly joined to the above-mentioned circuit board by the center section of this element side side by side to a single tier It is located in the above-mentioned element side at the both sides whose above-mentioned electrodes were pinched, at least one auxiliary electrode is arranged, and it is characterized by forming the bump joined to these auxiliary electrodes by the above-mentioned circuit board.
[0014] According to this composition, the bump who becomes the pillar which supports a semiconductor device to this auxiliary electrode can be formed in an element side by arranging an auxiliary electrode. For this reason, when a semiconductor device is mounted in the circuit board, in spite of adopting the so-called LOC structure which the posture of this semiconductor device was stabilized and arranged the electrode in the single tier in the center section of the element side, flip chip bonding of this semiconductor device can be easily carried out to the circuit board.
[0015] the circuit module indicated by the claim 6 in order to attain the above-mentioned purpose -- the circuit board and; -- it was mounted in this circuit board, and while having the element side which faces the above-mentioned circuit board, it has the semiconductor device and; which have arranged two or more electrodes directly joined to the above-mentioned circuit board by the center section of this element side side by side to the single tier
[0016] And it is characterized by having been located in the element side of the above-mentioned semiconductor device at the both sides whose above-mentioned electrodes were pinched, and having arranged at least one support salient which touches the above-mentioned circuit board. Since the support salient located in the both sides whose electrodes were pinched serves as a kind of pillar supporting a semiconductor device according to this composition, when a semiconductor device is mounted in the circuit board, the posture of this semiconductor device is stabilized. Therefore, flip chip bonding of the semiconductor device can be easily carried out to the circuit board, and high-density mounting can be realized.
[0017]
[Embodiments of the Invention] The gestalt of operation of the 1st of this invention is explained based on drawing 1 and drawing 2 below. Drawing 2 shows the circuit module 1 carried in electronic equipment like a portable computer. This circuit module 1 is equipped with the circuit board 2 and the semiconductor device 3 for memory mounted in this circuit board 2.
[0018] The semiconductor device 3 has the silicon base 4. The silicon base 4 has flat element side 4a which faces the circuit board 2, and this element side 4a is making the shape of a rectangle containing four corners 5a-5d.
[0019] As shown in drawing 1 , in the center section of element side 4a, many electrodes 7 consist, arrange an interval in a single tier, and each other are arranged. Element side 4a of this silicon base 4 is divided by 1st circuit area 8a and 2nd circuit area 8b by the above-mentioned electrode 7, and wiring made from aluminum which constitutes the LSI circuit which is not illustrated in these circuit area 8a and 8b is performed. This wiring is electrically connected to the above-mentioned electrode 7. Therefore, the above-mentioned semiconductor device 3 is making LOC structure.
[0020] Four auxiliary electrodes 10a-10d are arranged at screen 4a. Auxiliary electrodes 10a-10d have the same configuration and same size as the above-mentioned electrode 7, and are electrically connected to the above-mentioned wiring. These auxiliary electrodes 10a-10d are arranged at four corners 5a-5d of screen 4a, and buckling of track to the 1st and 2nd circuit area 8a and 8b is stopped few as much as possible.
[0021] Therefore, it has distributed the 1st or 4th auxiliary electrode 10a-10d at a time to two both sides whose electrodes 7 were pinched, and it has the physical relationship of a square vertex and these auxiliary electrodes 10a-10d are arranged, as a two-dot chain line shows to drawing 1 .
[0022] The ball-like solder bump 11 is formed in each electrode 7. Moreover, the solder bump 12 of the shape of a ball as a support salient is formed in auxiliary electrodes 10a-10d. These solder bumps 11 and 12 have the same configuration and the same size mutually.
[0023] As shown in drawing 2 , the above-mentioned circuit board 2 has many pads 14 into the mounting portion of a semiconductor device 3. A pad 14 corresponds to the above-mentioned solder bumps 11 and 12, and the solder bumps 11 and 12 are soldered to these pads 14. Therefore, flip chip bonding of the semiconductor device 3 is carried out to the circuit board 2, and it serves as a kind of pillar with which the solder ball 12 of four corners 5a-5d of the element side 4a supports a semiconductor device 3.
[0024] In addition, in the form of this operation, it fills up with adhesives 15 between element side 4a of a semiconductor device 3, and the circuit board 2, and a part for the connection of the solder balls 11 and 12 and a pad 14 is reinforced by these adhesives 15.
[0025] Since according to such composition auxiliary electrodes 10a-10d are arranged to four corners 5a-5d of element side 4a of a semiconductor device 3 and the solder bump 12 was formed in these auxiliary electrodes 10a-10d, where a semiconductor device 3 is mounted in the circuit board 2, the solder ball 12 functions as a pillar supporting the periphery of a semiconductor device 3. Therefore, a semiconductor device 3 will be supported by the circuit board 2 in four places of not only the electrode 7 of the center section of the element side 4a but the periphery of element side 4a.
[0026] Therefore, the mounting posture of the semiconductor device 3 to the circuit board 2 is stabilized, and in spite of

having adopted the LOC structure which arranged the electrode 7 in the single tier in the center section of element side 4a, flip chip bonding of this semiconductor device 3 can be easily carried out to the circuit board 2.
[0027] Consequently, the area which occupies the circuit board 2 compared with the conventional package decreases, and higher-density mounting is attained. Moreover, since the solder bump 12 supporting the above-mentioned semiconductor device 3 is located in the 1st of element side 4a, or the 4th corner 5a-5d, she can stop buckling of track to the 1st and 2nd circuit area 8a and 8b where wiring of an LSI circuit is performed few as much as possible. Therefore, the merit of the original LOC structure where the 1st and 2nd circuit area 8a and 8b is fully securable does not need to be spoiled.
[0028] Furthermore, since it connects with wiring of the silicon base 4 like the electrode 7, the 1st or 4th auxiliary electrode 10a-10d can distribute and arrange electrode section to the 1st of element side 4a, or the 4th corner 5a-5d. Therefore, the number of the electrodes 7 arranged in the center section of element side 4a can be reduced, the arrangement interval can be extended, and workability when carrying out flip chip bonding of the semiconductor device 3 to the circuit board 2 can be improved.
[0029] In addition, this invention is not specified as the gestalt of implementation of the above 1st, and shows the gestalt of operation of the 2nd of this invention to drawing 3 . With the gestalt of this 2nd operation, the 2nd and 4th auxiliary electrodes 10b and 10d are arranged in the center section of the longitudinal direction in the both-sides section whose electrode 7 of element side 4a was pinched. Therefore, as a two-dot chain line shows to drawing 3 , the 1st or 4th auxiliary electrode 10a-10d has a relation which is located at the peak of a parallelogram, and is arranged.
[0030] Also in such composition, a semiconductor device 3 can be supported by four places of the periphery of element side 4a, and the posture of a semiconductor device 3 is stabilized. Moreover, drawing 4 is indicating the form of operation of the 3rd of this invention.
[0031] The gestalt of this 3rd operation arranges the 1st or 3rd three auxiliary electrode 10a-10c to element side 4a. 1st auxiliary-electrode 10a is arranged in the center section of the longitudinal direction in the unilateral section of element side 4a. The 2nd and 3rd auxiliary electrodes 10b and 10c are arranged with 1st auxiliary-electrode 10a at the 2nd and 3rd corners 5b and 5c located in the opposite side whose electrode 7 was pinched. And as a two-dot chain line shows to drawing 4 , the 1st or 3rd auxiliary-electrode 10a has a relation which is located at a triangular vertex, and is arranged.
[0032] According to such composition, the periphery of element side 4a of a semiconductor device 3 can be supported in the position of a triangular vertex, and the posture of a semiconductor device 3 is stabilized. Drawing 5 is indicating the gestalt of operation of the 4th of this invention.
[0033] With the gestalt of this 4th operation, 1st auxiliary-electrode 10a is arranged at 1st corner 5a of element side 4a, and the other composition is the same as that of the gestalt of implementation of the above 3rd. Also in this composition, the periphery of element side 4a of a semiconductor device 3 can be supported by the physical relationship of a triangular vertex, and the posture of a semiconductor device 3 is stabilized.
[0034] Furthermore, drawing 6 is indicating the gestalt of operation of the 5th of this invention. The gestalt of this 5th operation arranges two auxiliary electrodes, the 1st and the 2nd, 10a and 10b to element side 4a. 1st auxiliary-electrode 10a is arranged at 1st corner 5a of element side 4a, and 2nd auxiliary-electrode 10b is arranged at 2nd corner 5b of element side 4a. These [1st] and the 2nd auxiliary electrode 10a and 10b face mutually on both sides of the electrode 7 in the end section in alignment with the longitudinal direction of element side 4a. Therefore, as a two-dot chain line shows to drawing 6 , the electrode 7 to which the 1st and 2nd auxiliary electrodes 10a and 10b and these auxiliary electrodes 10a and 10b are located in the edge of an opposite side has a relation which is located at a triangular vertex, and it is arranged.
[0035] According to such composition, a semiconductor device 3 is supportable by three places of the periphery of element side 4a. Therefore, while being stabilized and being able to support a semiconductor device 3 by two auxiliary electrodes, the 1st and the 2nd, 10a and 10b, it can use as the 1st and 2nd extended area 8a and 8b to the 3rd of element side 4a, and corner 4th / 5c and 5d] all the corners.
[0036] Moreover, drawing 7 is indicating the gestalt of operation of the 6th of this invention. With the gestalt of this 6th operation, the 1st and 2nd auxiliary electrodes 10a and 10b are arranged in the center section of the longitudinal direction in the both-sides section of element side 4a which counters each other on both sides of an electrode 7.
[0037] According to this composition, the 1st and 2nd auxiliary electrodes 10a and 10b and the electrode 7 of ends serve as a relation which is located at a square vertex, as a two-dot chain line shows to drawing 7 , and they can support a semiconductor device 3 by four places of the periphery of element side 4a. Therefore, like the form of implementation of the above 5th, only by adding two auxiliary electrodes, the 1st and the 2nd, 10a and 10b, it is stabilized and a semiconductor device 3 can be supported.
[0038] With it, it can use as the 1st and 2nd extended area 8a and 8b to the 1st of element side 4a, or corner [4th / 5a-5d] all the corners, and the merit of original of LOC structure can fully be employed efficiently.
[0039] In addition, although the solder bump was formed in the auxiliary electrode which has an electric flow function with the gestalt of each above-mentioned implementation, the above-mentioned auxiliary electrode may be used as the so-called dummy electrode which does not have an electric flow function, and a solder bump may be formed in these dummy electrode.
[0040] Moreover, a solder bump's configuration may not be specified in the shape of a ball, either, for example, you may have the shape of the shape of a mushroom, and a pin. Furthermore, although the solder bump was formed in the auxiliary electrode and this solder bump was used as a support salient in the above-mentioned example, this invention is giving plating of gold, copper, nickel, or solder to an auxiliary electrode not only instead of this but instead of a solder bump, and it carries out the laminating of the deposit on this auxiliary electrode, and you may make it use this deposit as a support salient. Even if it

makes it the electrode of a semiconductor device, it is not specified as what is joined to the pad on the circuit board through a solder bump, but it replaces with this solder bump, a deposit is formed, and you may make it similarly solder this deposit to the pad on the circuit board.

[0041] Moreover, instead, a wire bonder is used for an electrode and an auxiliary electrode, a golden bump is formed in a solder bump's, and you may make it solder this golden bump to the pad on the circuit board.

[0042]

[Effect of the Invention] Since the support salient of the both sides whose electrodes were pinched functions as a kind of pillar supporting a semiconductor device according to this invention explained in full detail above, the posture of this semiconductor device is stabilized and flip chip bonding of the semiconductor device of LOC structure can be easily carried out to the circuit board. Therefore, there is little area which occupies the circuit board compared with the conventional package, and it ends, and higher-density mounting of it is attained.

[Translation done.]

CLAIMS

[Claim(s)]
[Claim 1] The semiconductor device characterized by having had the element side which faces the circuit board, being the semiconductor device which has arranged two or more electrodes directly joined to the above-mentioned circuit board by the center section of this element side side by side to the single tier, having been located in the both sides whose above-mentioned electrodes the above-mentioned element side pinched, and having arranged at least one support salient which touches the above-mentioned circuit board.
[Claim 2] It is the semiconductor device characterized by for the above-mentioned element side having four corners in the publication of a claim 1, and arranging the support salient at these corners, respectively.
[Claim 3] It is the semiconductor device characterized by for the above-mentioned support salient having a relation which is located at a triangular vertex when the above-mentioned element side is seen superficially in the publication of a claim 1, and being arranged.
[Claim 4] It is the semiconductor device characterized by the above-mentioned support salient serving as the function as an electrode in the publication of a claim 1.
[Claim 5] The semiconductor device characterized by forming the bump who has the element side which faces the circuit board, is the semiconductor device which has arranged two or more electrodes directly joined to the above-mentioned circuit board by the center section of this element side side by side to the single tier, is located in the both sides whose above-mentioned electrodes the above-mentioned element side pinched, arranges at least one auxiliary electrode, and is joined to these auxiliary electrodes by the above-mentioned circuit board.
[Claim 6] The circuit board; the circuit module characterized by to have been mounted in this circuit board, to be a circuit module equipped with the semiconductor device which has arranged two or more electrodes directly joined to the above-mentioned circuit board by the center section of this element side side by side to the single tier while having the element side which faces the above-mentioned circuit board, and;, to have been located in the both sides whose above-mentioned electrodes the element side of the above-mentioned semiconductor device pinched, and to have arranged at least one support salient which touches the above-mentioned circuit board.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The perspective diagram of the semiconductor device concerning the gestalt of operation of the 1st of this invention.
[Drawing 2] The cross section of the circuit module in which the state where the semiconductor device was mounted in the circuit board is shown.
[Drawing 3] The perspective diagram of the semiconductor device concerning the gestalt of operation of the 2nd of this invention.
[Drawing 4] The perspective diagram of the semiconductor device concerning the gestalt of operation of the 3rd of this invention.
[Drawing 5] The perspective diagram of the semiconductor device concerning the gestalt of operation of the 4th of this invention.
[Drawing 6] The perspective diagram of the semiconductor device concerning the gestalt of operation of the 5th of this invention.
[Drawing 7] The perspective diagram of the semiconductor device concerning the gestalt of operation of the 6th of this invention.
[Description of Notations]
1 -- Circuit module
2 -- Circuit board
3 -- Semiconductor device
4a -- Element side
7 -- Electrode
12 -- Support salient (solder bump)

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] this invention is related at the semiconductor device which makes connection between the electrode of a semiconductor chip, and the mounting pad of a wiring substrate using relation of connection between a semiconductor chip and a wiring substrate, and flip chip mounting especially using the pewter to connection between a semiconductor chip and a wiring substrate.
[0002]
[Description of the Prior Art] In the semiconductor device using flip chip mounting of the conventional technology, when connecting a semiconductor chip and a wiring substrate, in order to keep uniform the interval size when connecting of a semiconductor chip and a wiring substrate, JP,7-226422,A etc. is raised as a semiconductor device which used the spacer.
[0003] The conventional spacer is formed and the structure of the semiconductor device using flip chip mounting is explained using drawing 13 and drawing 14 .
[0004] Drawing 13 and drawing 14 are the cross sections showing the semiconductor device indicated by above-mentioned JP,7-226422,A. The structure of drawing 13 is explained. On the semiconductor chip 21, the salient electrode 22 and spacer 23 which are fused at predetermined temperature are formed, and the small small salient 26 of a path is formed at the nose of cam of a spacer 23 rather than the spacer 23. A through hole 27 is formation ******** so that the pad section 24 may be formed in the wiring substrate 25 so that it may correspond to arrangement of the salient electrode 22 of a semiconductor chip 21, and it may correspond to arrangement of the small salient 26 of a spacer 23. A semiconductor chip 21 and the wiring substrate 25 perform electrical installation by the salient electrode 22 formed in the semiconductor chip 21, the small salient 26 of a spacer 23 is inserted in the through hole 27 of the wiring substrate 25, and the semiconductor chip 21 and the wiring substrate 25 are positioned.
[0005] The structure of drawing 14 is explained. On the semiconductor chip 21, the salient electrode 22 and spacer 23 which are fused at predetermined temperature are formed. The pad section 24 is formed in the wiring substrate 25 so that it may correspond to arrangement of the salient electrode 22 of a semiconductor chip 21, and the level difference 28 for regulating the position of a spacer 23 is formed. A semiconductor chip 21 and the wiring substrate 25 perform electrical installation by the salient electrode 22 formed in the semiconductor chip 21, a spacer 23 is contacted on the side to the level difference 28 of the wiring substrate 25, and the semiconductor chip 21 and the wiring substrate 25 are positioned.
[0006]
[Problem(s) to be Solved by the Invention] however, when the spacer which prepared the hole or the level difference in the wiring substrate, and was formed in the semiconductor chip side is positioned and the position gap with the electrode pad of a wiring substrate, a hole, or a level difference occurs, a salient electrode and electrode Bud are slanting like drawing 15 -- it will join By this, the stress to the connection generated by supplying to environmental tests, such as a heat cycle test, will concentrate, and the thermal-fatigue life of a semiconductor device will fall. Moreover, when position gap exceeds connection tolerance, that a salient electrode and electrode Bud cannot connect occurs.
[0007] (The purpose of invention) The purpose of this invention is to offer the formation method of the semiconductor semiconductor device which can keep the interval of a semiconductor chip and a wiring substrate constant, and a spacer, even if it solves the above-mentioned technical problem and the position gap with a mounting pad and a salient electrode occurs.
[0008]
[Means for Solving the Problem] In order to attain the purpose mentioned above, the structure of the semiconductor device of this invention and the manufacture method of a spacer adopt the composition of the following publication.
[0009] One semiconductor device of this invention is characterized by forming a low spacer and making connection only with other electric salient electrodes to them rather than it, or it is the same as the height of other salient electrodes to at least three places in the semiconductor device which connects a semiconductor chip through a salient electrode on a wiring substrate.
[0010] Or another semiconductor device of this invention is the same as the height of the salient electrode currently formed in at least three places on a wiring substrate in the semiconductor device which connects a semiconductor chip through a salient electrode at the semiconductor chip at the wiring substrate top, it is characterized by forming a low spacer and making connection only with the electric salient electrode of the semiconductor chip of ** rather than it.
[0011]
[Embodiments of the Invention] Hereafter, composition of the semiconductor device in the 1st operation gestalt of this

invention is explained using a drawing. About the 1st operation gestalt of this invention, structure is explained using drawing 1 - drawing 3 . The plan by the side of the electrode of a semiconductor chip 1 and drawing 3 of the cross section of a semiconductor device [in / the 1st operation gestalt of this invention / in drawing 1] and drawing 2 are the plans by the side of semiconductor chip mounting of a wiring substrate.

[0012] A semiconductor chip 1 is explained using drawing 2 . An electronic circuitry is formed on Si and the electrode is formed with aluminum etc. as an external terminal of the circuit. In order to perform electrical installation with the electrode pad 6 of the wiring substrate 5 on an electrode, the ratio of Sn and Pb forms the salient electrode 1 with the pewter of composition of 6:4.

[0013] About the spacer 3, the resin material whose 5Sn / 95Pb high-melting point pewter, or coefficient of linear expansion which is a refractory metal is 20-30 ppm/degree C is used rather than the salient electrode 2.

[0014] The salient electrode 2 of a semiconductor chip 1 and portions other than spacer 3 are further covered by the inorganic film of inorganic films, such as SiN, by the protective coat by organic films, such as a polyimide, on it, and the exterior is insulated electrically.

[0015] The wiring substrate 5 is explained using drawing 3 . When a wiring substrate is a resin substrate, the alumina etc. is used for the case at the base material at the ceramic substrate using glass epoxy, BT resin, the polyimide, etc. The pad section 4 of the wiring substrate 5 is formed so that it may correspond to arrangement of the salient electrode 2 currently formed in a semiconductor chip 1.

[0016] The pad section 4 has given Au/nickel plating on Cu, in order for the salient electrode 2 formed with the eutectic pewter of a semiconductor chip 1 to fully get wet and to secure sufficient adhesion intensity. As for metal layer thickness, nickel layer thickness forms 3-5 micrometers and Au layer thickness by 0.02-0.05 micrometers, respectively.

[0017] Two kinds of pad sections 7 for spacers are considered by setup of the height of the salient electrode 2 and a spacer 3. In many cases, the pad section 7 for spacers is formed as shown in drawing 4 (1) or (2). In this case, the height of the salient electrode 2 and a spacer 3 is made the same. However, when opening cannot be carried out to a solder resist 6 by leading about of wiring of the case where the interval of the salient electrode 2 and a spacer 3 is narrow, or the wiring substrate 5, the pad section of a spacer is formed like drawing 5 . In this case, from the height of the salient electrode 2, the spacer 3 height of a semiconductor chip 1 is low set up by the thickness of a solder resist 6, and is needed.

[0018] The portion is covered by the solder resist 6 except the pad section 4 of the above [the wiring substrate 5], and pad section 7 for spacers.

[0019] A semiconductor device is explained to be the above-mentioned semiconductor chip 1 using drawing 1 including the wiring substrate 5. The electrical installation of each salient electrode 2 on a semiconductor chip 1 and the pad section 4 on the wiring substrate 5 fuses the pewter of the salient electrode 2, and connects with the salient electrode 2 as the pad section 4. The semiconductor chip 1, the wiring substrate 5, and interval in that case are decided by the height of a spacer 3, and always stabilized mounting is attained, without inclining.

[0020] Between a semiconductor chip 1 and the wiring substrate 5, it is closing by the closure resin 8 for protection of the circuit currently formed in the improvement in reliability, the semiconductor chip 1, and the wiring substrate 5 of a connection. The thermosetting epoxy system resin is used for the closure resin 8.

[0021] About the 2nd operation gestalt of this invention, structure is explained using drawing 6 - drawing 8 . The plan by the side of the electrode of a semiconductor chip 1 and drawing 3 of the cross section of a semiconductor device [in / the 2nd operation gestalt of this invention / in drawing 6] and drawing 7 are the plans by the side of semiconductor chip mounting of a wiring substrate.

[0022] A semiconductor chip 1 is explained using drawing 7 . An electronic circuitry is formed on Si and the electrode is formed with aluminum etc. as an external terminal of the circuit. In order to perform electrical installation with the electrode pad 6 of the wiring substrate 5 on an electrode, the ratio of Sn and Pb forms the salient electrode 1 with the pewter of composition of 6:4.

[0023] About the pad section 11 for spacers, it is formed by Cu, Au, etc. equivalent to the best layer of the barrier metal layer at the time of forming aluminum and the salient electrode which are the electrode of IC, and the same material as wiring.

[0024] The salient electrode 2 of a semiconductor chip 1 and portions other than pad section 11 for spacers are further covered by inorganic films or the aforementioned inorganic films, such as SiN, by the protective coat by organic films, such as a polyimide, on it, and the exterior is insulated electrically.

[0025] The wiring substrate 5 is explained using drawing 8 . Glass epoxy, BT resin, the polyimide, etc. are used for the base material of a wiring substrate. The pad section 4 of the wiring substrate 5 is formed so that it may correspond to arrangement of the salient electrode 2 currently formed in a semiconductor chip 1.

[0026] The pad section 4 has given Au/nickel plating on Cu, in order for the salient electrode 2 formed with the eutectic pewter of a semiconductor chip 1 to fully get wet and to secure sufficient adhesion intensity. As for each metal layer thickness, nickel layer thickness forms 3-5 micrometers and Au layer thickness by 0.02-0.05 micrometers.

[0027] The resin material whose 5Sn / 95Pb high-melting point pewter, or coefficient of linear expansion which is a refractory metal is 20-30 ppm/degree C is used for the spacer 10 rather than the salient electrode 2.

[0028] About a setup of the height of a spacer 10, it is the same as the 1st operation gestalt, and height is formed according to the structure of the pad section 11 for spacers similarly to the salient electrode 2 lower than the salient electrode 2.

[0029] The portion is covered by the solder resist 6 except pad section [of the above / the wiring substrate 5] 4, and spacer 10.

[0030] A semiconductor device is explained to be the above-mentioned semiconductor chip 1 using drawing 6 including the wiring substrate 5. The electrical installation of each salient electrode 2 on a semiconductor chip 1 and the pad section 4 on the wiring substrate 5 fuses the pewter of the salient electrode 2, and connects the salient electrode 2 and the pad section 4. The semiconductor chip 1, the wiring substrate 5, and interval in that case are decided by the height of a spacer 10, and always stabilized mounting is attained, without inclining.
[0031] Between a semiconductor chip 1 and the wiring substrate 5, it is closing by the closure resin 8 for protection of the circuit currently formed in the improvement in reliability, the semiconductor chip 1, and the wiring substrate 5 of a connection. The thermosetting epoxy system resin is used for the closure resin 8.
[0032] The formation method of the spacer used for the 1st operation gestalt is explained. It explains using the drawing of drawing 9 - drawing 12 .
[0033] Drawing 9 is the cross section of a semiconductor chip 1. An electronic circuitry is formed on Si12 and the electrode 13 is formed with aluminum etc. as an external terminal of the circuit. Further, on it, portions other than electrode 14 are covered by the protective coat 14 by organic films, such as a polyimide, and are electrically insulated with the exterior by inorganic films or the aforementioned inorganic films, such as SiN.
[0034] the whole surface on a semiconductor chip -- the order of aluminum, Cr, and Cu -- or it forms by vacuum evaporationo or sputtering Furthermore, a resist is formed in the whole surface, and after [which removes resists other than the position which forms the independent electrode 15 for spacers in the field in which the electrode 14 and the semiconductor pad are not formed, uses a resist as a mask, and is depended on the sputtering method by the photolithography] carrying out dry etching and removing, an electrode 14 and the electrode 15 for spacers are formed like drawing 10 by removing a resist with resist ablation liquid further.
[0035] Drawing 11 expresses the state where the spacer was formed. When forming the spacer of 5Sn / 95Pb high-melting point pewter which is a refractory metal, a resist is applied to the whole surface, and opening is carried out, and by non-electrolyzed pewter plating, only the electrode 15 for spacers forms the spacer 15 of 5Sn / 95Pb high-melting point pewter, and exfoliates a resist.
[0036] When forming the spacer of a resin, a postcure is formed and carried out by the heat-hardened type resin of the height which accepted electrode 15 and was set up for spacers with screen printing, and a spacer is formed.
[0037] up to the temperature which supplies a eutectic pewter ball with a replica method after supplying a eutectic pewter paste with screen printing or applying hyperviscous flux only to an electrode 14 in order to form the salient electrode 2 as drawing 12 shows after that, and a eutectic pewter fuses at a reflow furnace etc. -- heating -- an electrode 14 top -- the salient electrode of a eutectic pewter -- it forms two times
[0038] The formation method spacer which the 1st operation gestalt used also about the formation method of the spacer used for the 2nd operation gestalt next is formed.
[0039]
[Effect of the Invention] In the semiconductor device which connects a semiconductor chip through a salient electrode on a wiring substrate, as explained above, or it is the same as the height of other salient electrodes to at least three places, rather than it, the low spacer was formed and only the salient electrode has connected with them. Even if the position gap with a mounting pad and a salient electrode occurs by this, it is lost with a spacer that a salient electrode and electrode Bud join aslant. A thermal-fatigue life is stabilized by the semiconductor device by this.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the cross section showing the semiconductor device in the 1st operation gestalt of this invention.
[Drawing 2] It is the plan of the semiconductor chip in the 1st operation gestalt of this invention.
[Drawing 3] It is the plan of the wiring substrate in the 1st operation gestalt of this invention.
[Drawing 4] It is the cross section of the pad section for the spacers of the wiring substrate in the 1st operation gestalt of this invention.
[Drawing 5] It is the cross section of the pad section for the spacers of the wiring substrate in the 1st operation gestalt of this invention.
[Drawing 6] It is the cross section showing the semiconductor device in the 2nd operation gestalt of this invention.
[Drawing 7] It is the plan of the semiconductor chip in the 2nd operation gestalt of this invention.
[Drawing 8] It is the plan of the wiring substrate in the 2nd operation gestalt of this invention.
[Drawing 9] It is a semiconductor chip cross section in the formation method of the spacer of the 1st operation gestalt of this invention.
[Drawing 10] It is the cross section showing the state where the electrode for spacers was formed in the semiconductor chip in the formation method of the spacer of the 1st operation gestalt of this invention.
[Drawing 11] It is the cross section showing the state where the spacer was formed in the semiconductor chip in the formation method of the spacer of the 1st operation gestalt of this invention.
[Drawing 12] It is the cross section showing the state where the salient electrode was formed in the semiconductor chip in the formation method of the spacer of the 1st operation gestalt of this invention.
[Drawing 13] It is the cross section showing the semiconductor device in the conventional technology.
[Drawing 14] It is the cross section showing the semiconductor device in the conventional technology.
[Drawing 15] It is the cross section showing the connection of the semiconductor device in the conventional technology.
[Description of Notations]
1 Semiconductor Chip
2 Salient Electrode
3 Spacer
4 Pad Section
5 Wiring Substrate
6 Solder Resist
7 Spacer Pad Section
8 Closure Resin

[Translation done.]

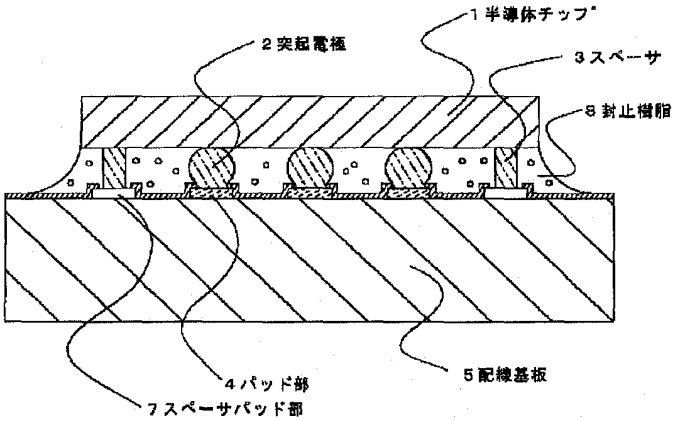
CLAIMS

[Claim(s)]
[Claim 1] The semiconductor device characterized by forming a low spacer and making connection only with other electric salient electrodes to them rather than it in the semiconductor device which connects a semiconductor chip through a salient electrode on a wiring substrate or it is the same as the height of other salient electrodes to at least three places.
[Claim 2] The semiconductor device with which material of a spacer was characterized by being a refractory metal rather than other salient electrodes in the semiconductor device according to claim 1.
[Claim 3] The semiconductor device characterized by the material of a spacer being resin material in the semiconductor device according to claim 1.
[Claim 4] The semiconductor device characterized by arranging in addition to the internal element formation circuit field of the semiconductor chip of the above [a spacer] in the semiconductor device according to claim 1. [Claim 5] The semiconductor device characterized by forming the electrode corresponding to the spacer of the aforementioned semiconductor chip in the wiring substrate in which the aforementioned semiconductor chip is carried in the semiconductor device according to claim 1.
[Claim 6] The semiconductor device characterized by forming a low spacer and making connection only with the electric salient electrode of the aforementioned semiconductor chip rather than it or it is the same as the height of the salient electrode currently formed in at least three places on a wiring substrate in the semiconductor device which connects a semiconductor chip through a salient electrode at the semiconductor chip at the wiring substrate top.
[Claim 7] The semiconductor device characterized by being a refractory metal rather than the salient electrode which the material of the spacer formed in a wiring substrate forms in a semiconductor chip in a semiconductor device according to claim 6.
[Claim 8] The semiconductor device characterized by the material of the spacer formed in a wiring substrate being resin material in the semiconductor device according to claim 6.
[Claim 9] The semiconductor device characterized by arranging in addition to the internal element formation circuit field of the aforementioned semiconductor chip when the spacer arrangement formed in a wiring substrate carries the aforementioned semiconductor chip in a wiring substrate in a semiconductor device according to claim 6.
[Claim 10] The semiconductor device characterized by forming the electrode corresponding to the spacer of a wiring substrate in the aforementioned semiconductor chip in the semiconductor device according to claim 6.
[Claim 11] The spacer formation method characterized by having the process which forms the spacer of a refractory metal from the salient electrode formed in other electrodes in the process which forms other electrodes and the independent electrode which has not connected electrically in the field which does not form the pad of a semiconductor chip, other electrodes, and the independent electrode which has not connected electrically.
[Claim 12] The spacer formation method characterized by having the process which forms the spacer of a resin in the process which forms other electrodes and the independent electrode which has not connected electrically in the field which does not form the pad of a semiconductor chip, other electrodes, and the independent electrode which has not connected electrically.

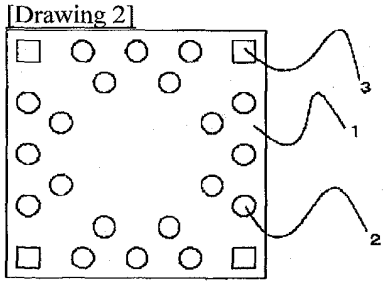
[Translation done.]

DRAWINGS

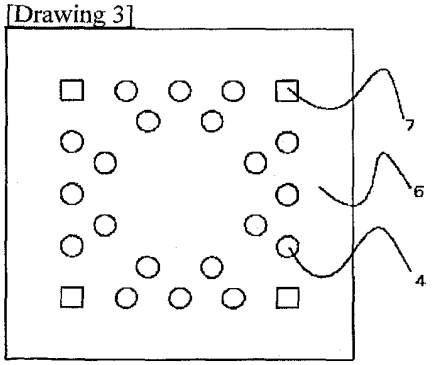
[Drawing 1]



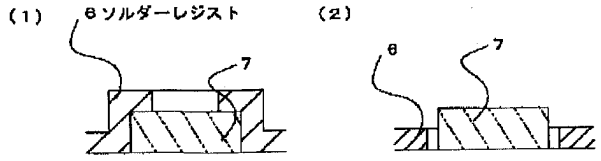
[Drawing 2]



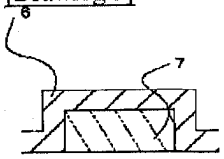
[Drawing 3]



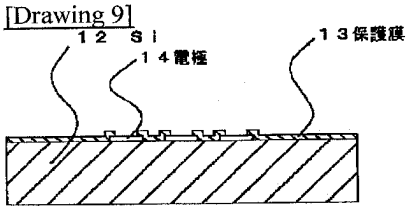
[Drawing 4]



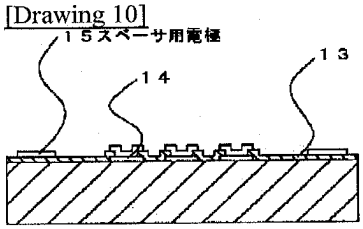
[Drawing 5]



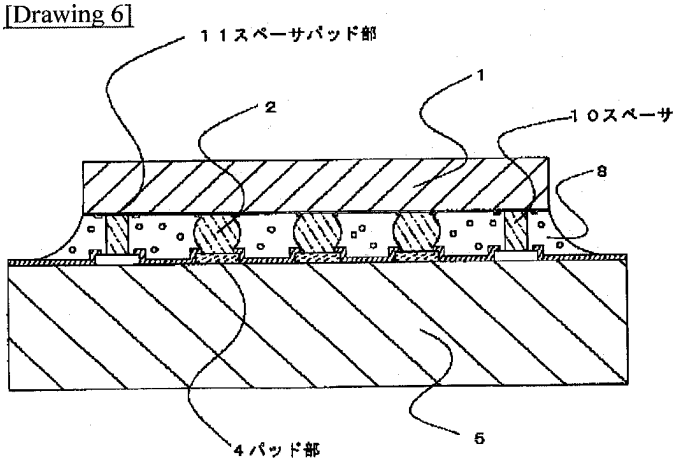
[Drawing 9]



[Drawing 10]



[Drawing 6]



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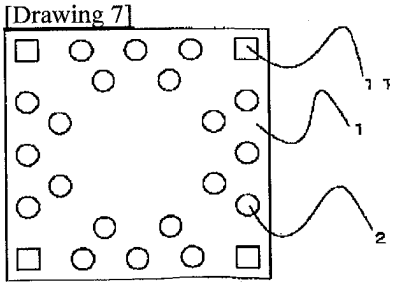
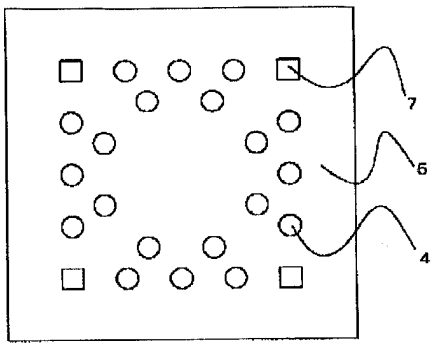
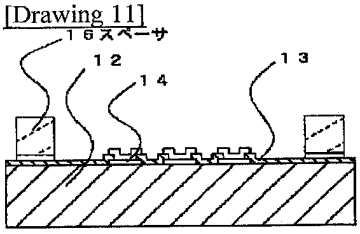


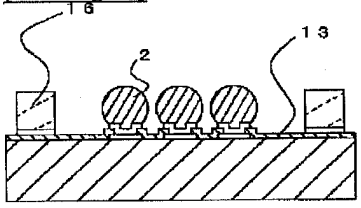
[Drawing 8]



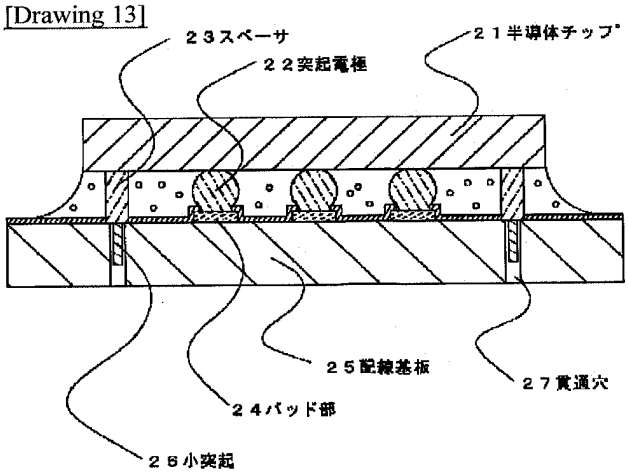
[Drawing 11]



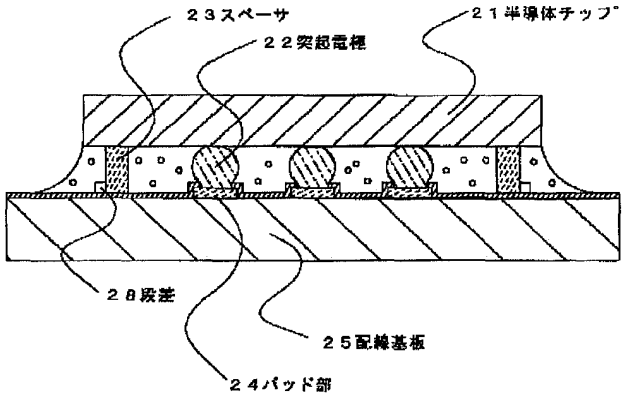
[Drawing 12]



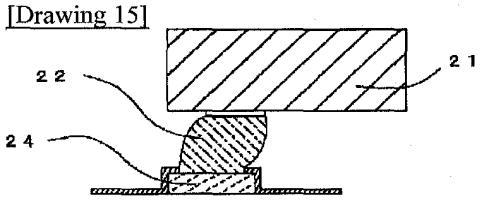
[Drawing 13]



[Drawing 14]



[Drawing 15]



[Translation done.]